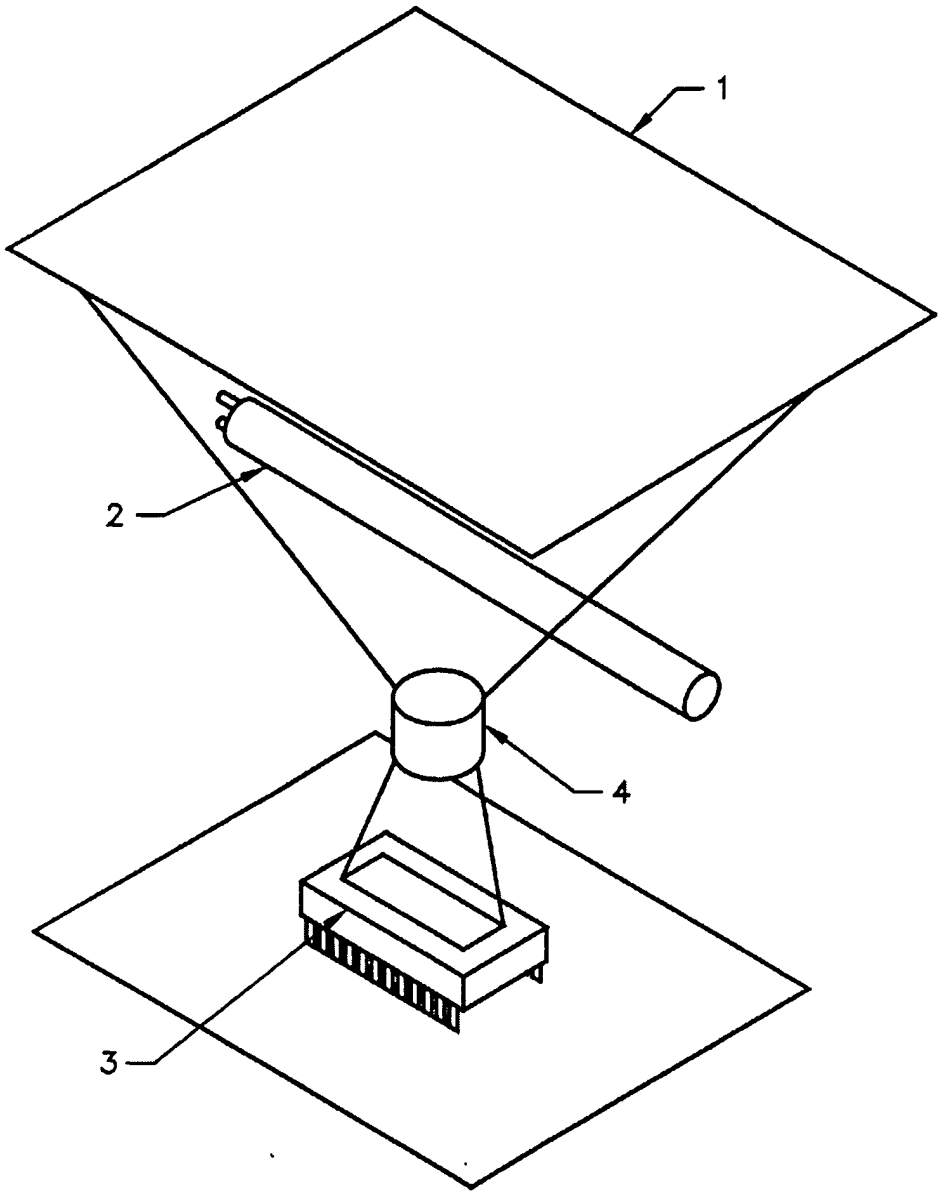

FIG. 1
(PRIOR ART)

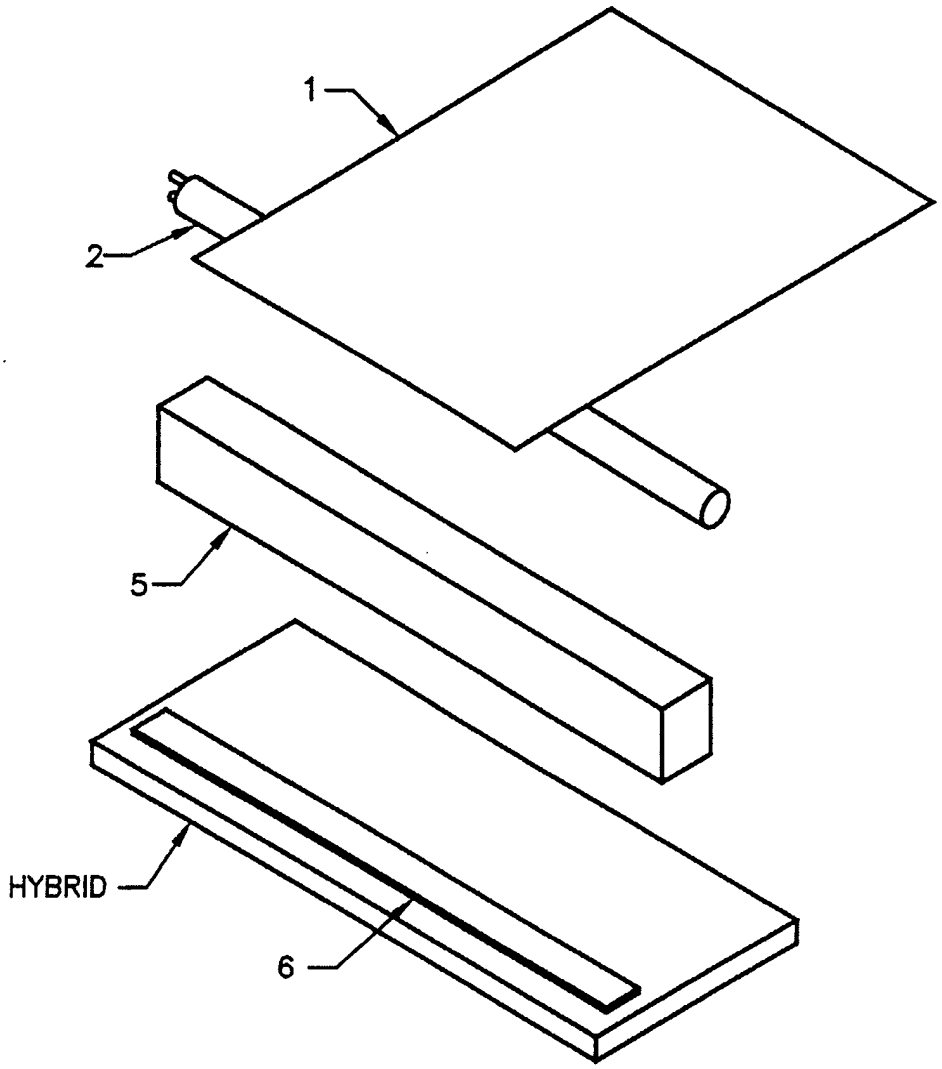

FIG. 2
(PRIOR ART)

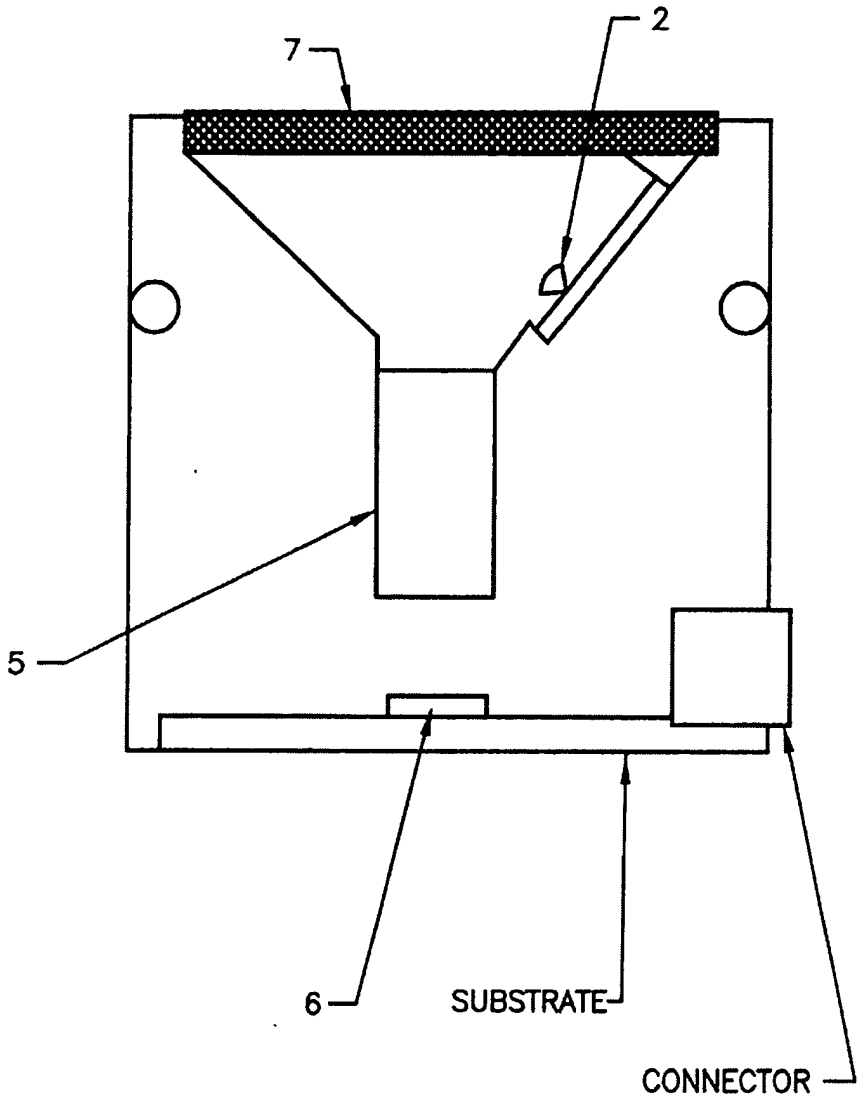

FIG. 3
(PRIOR ART)

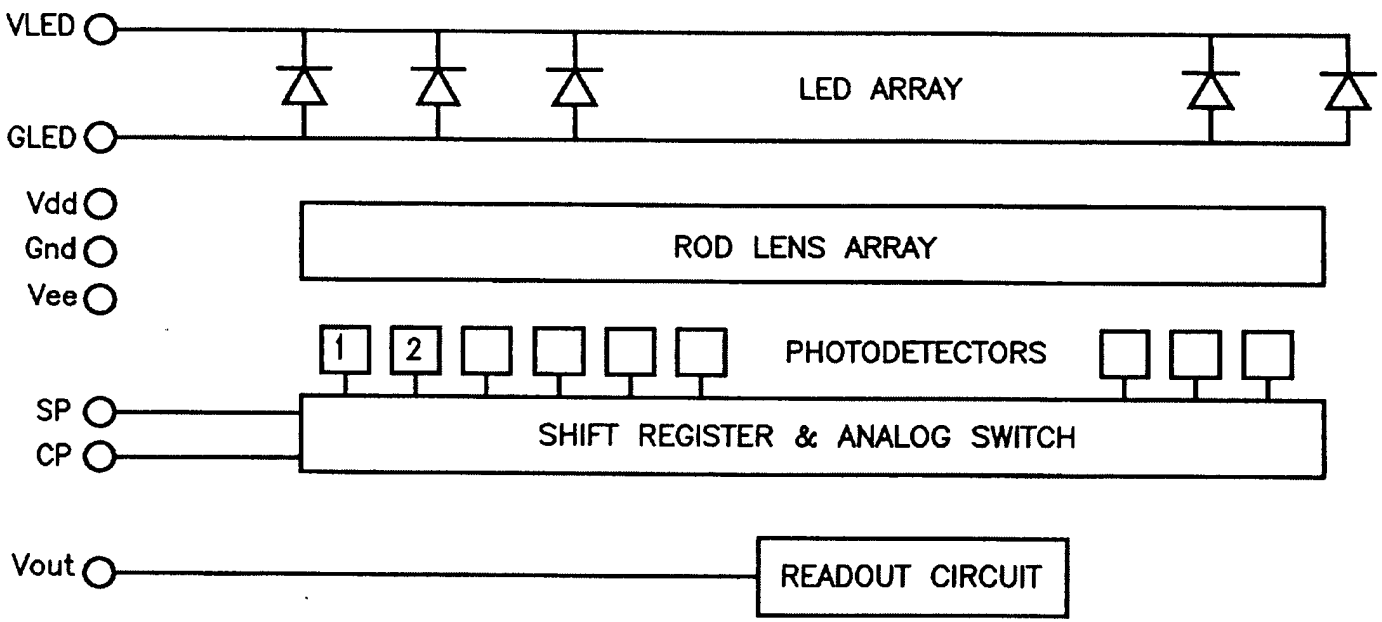

FIG. 4
(PRIOR ART)

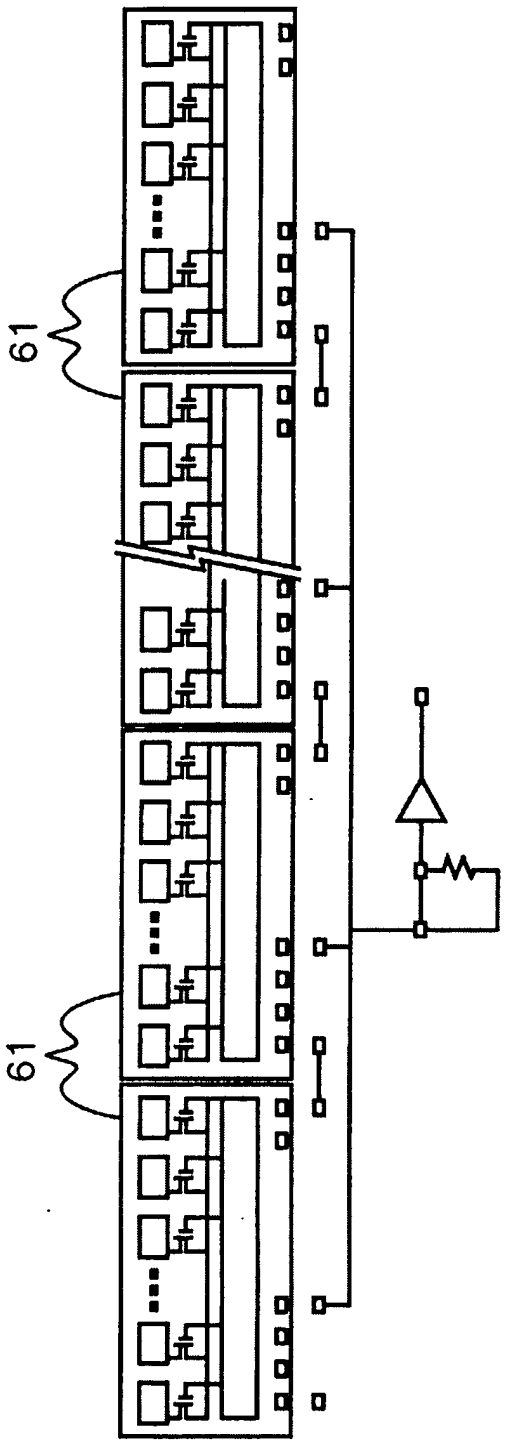

FIG. 5
(PRIOR ART)

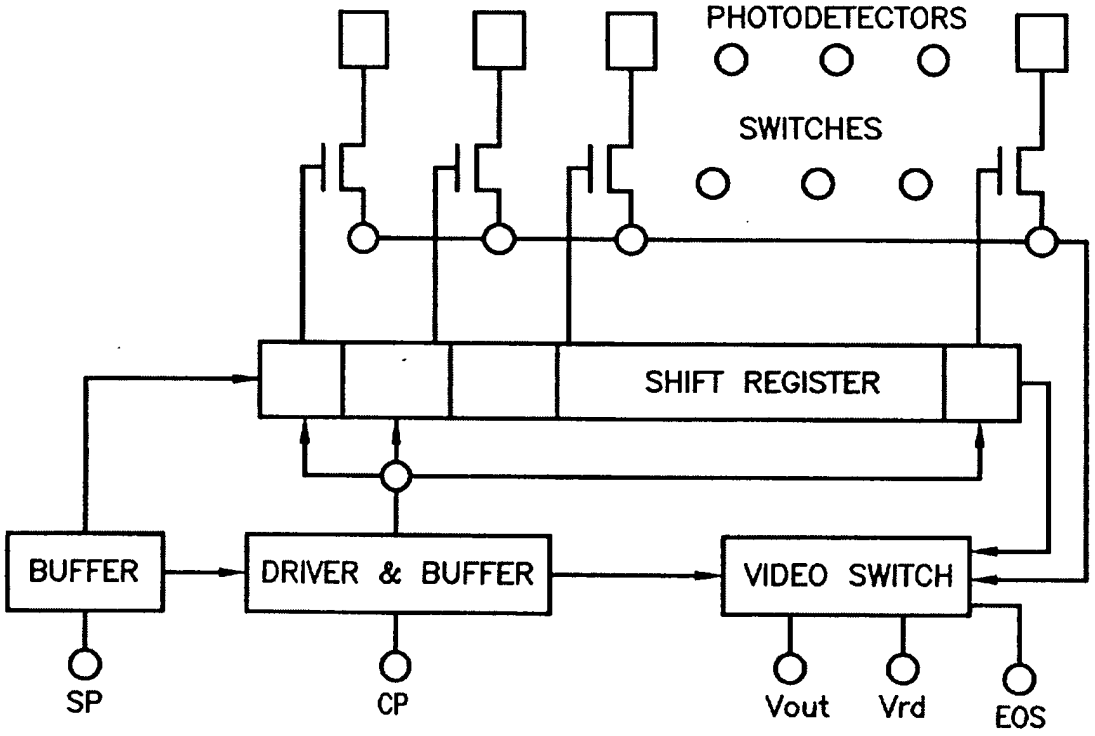

FIG. 6
(PRIOR ART)

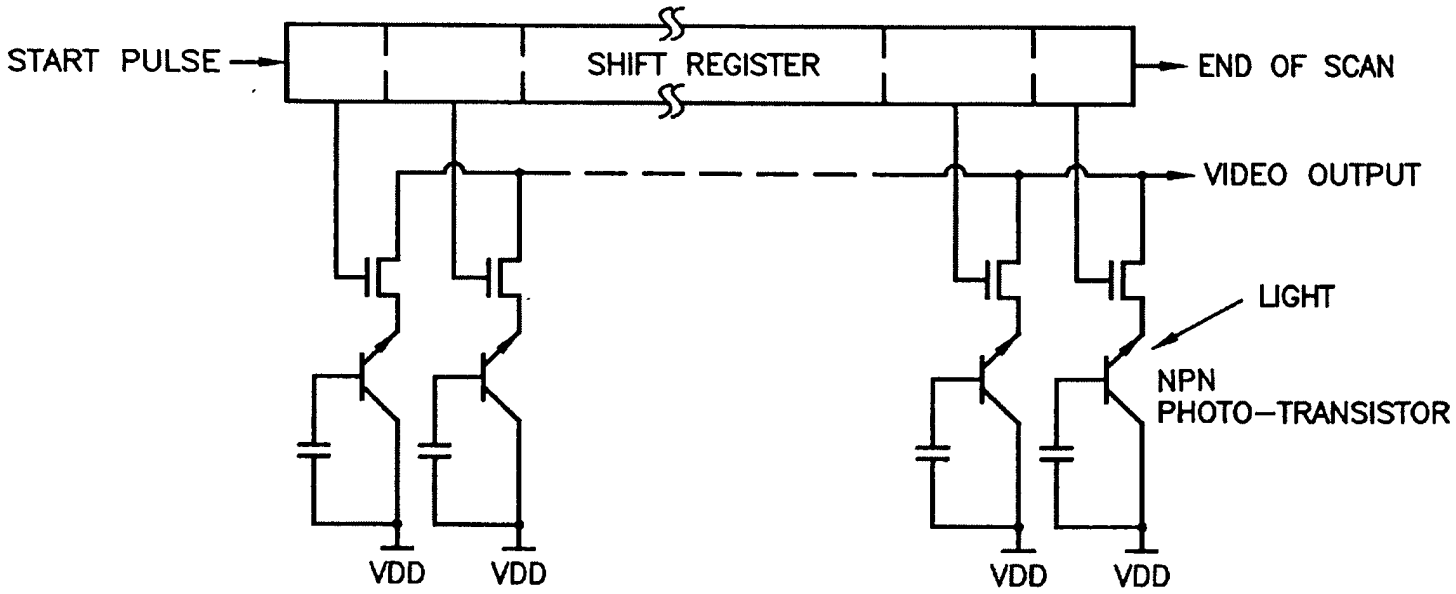

FIG. 7
(PRIOR ART)

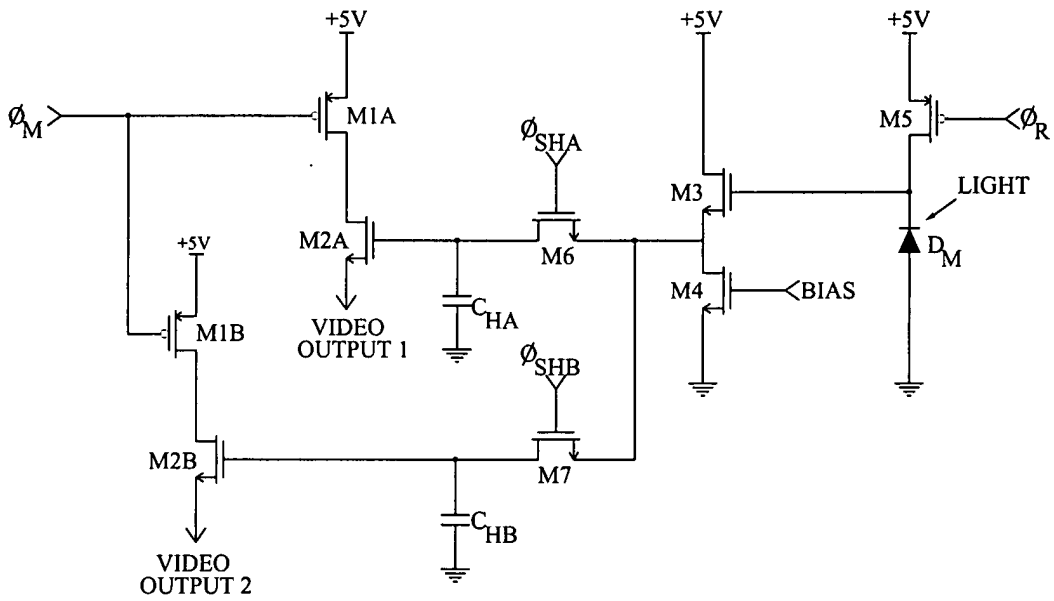

FIG. 8
(PRIOR ART)

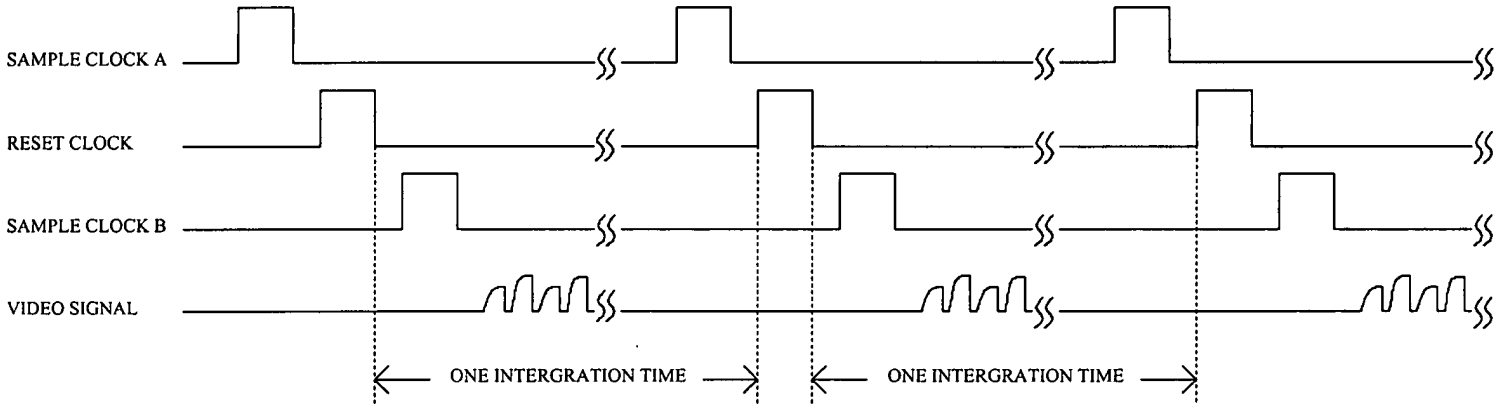

FIG. 9A NON-CDS OPERATION TIMING
(PRIOR ART)

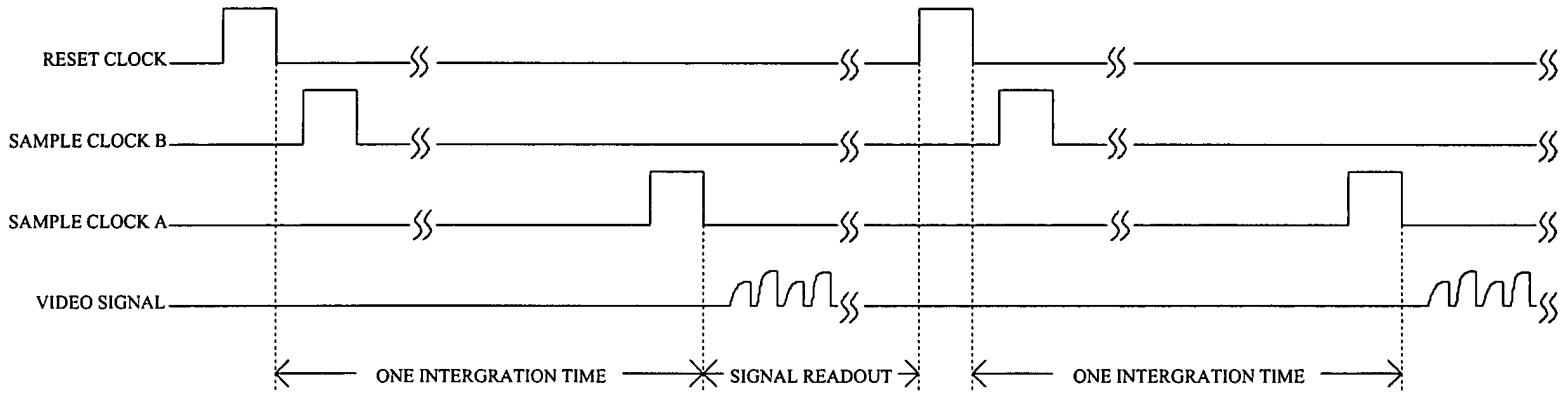

FIG. 9B CDS OPERATION TIMING
(PRIOR ART)

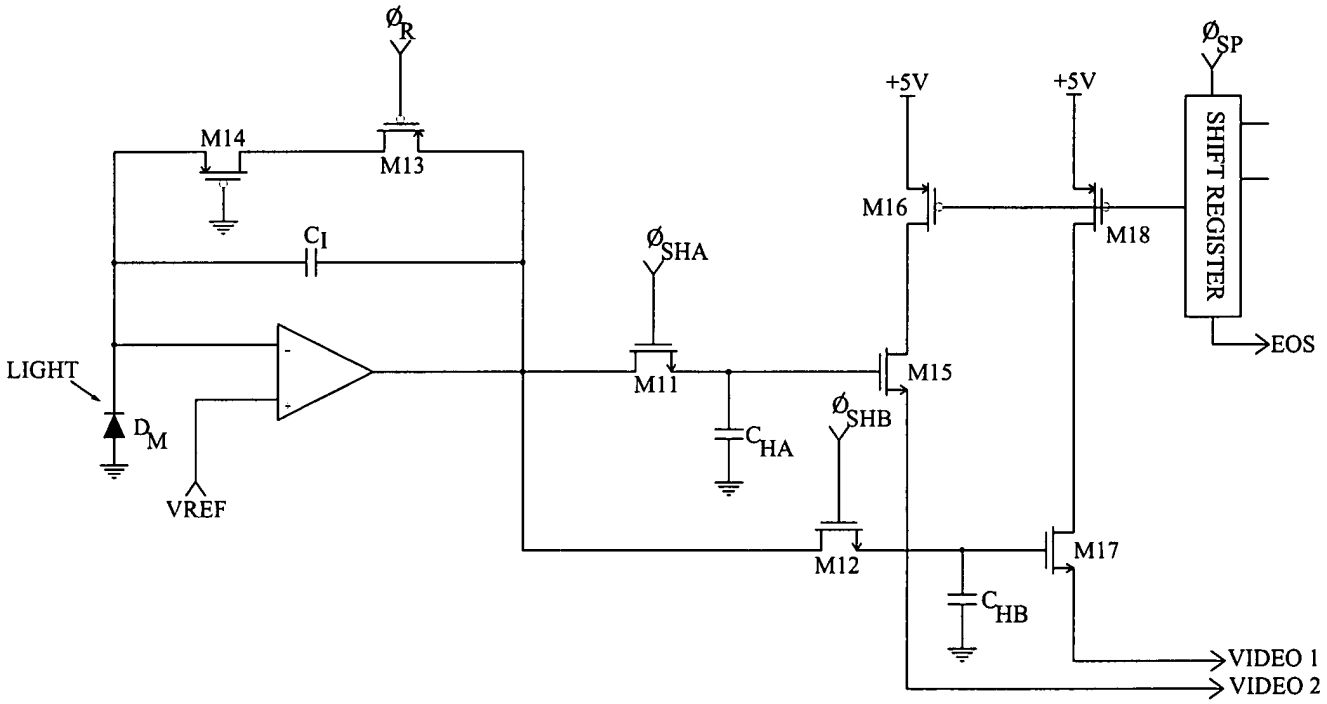

FIG. 10
(PRIOR ART)

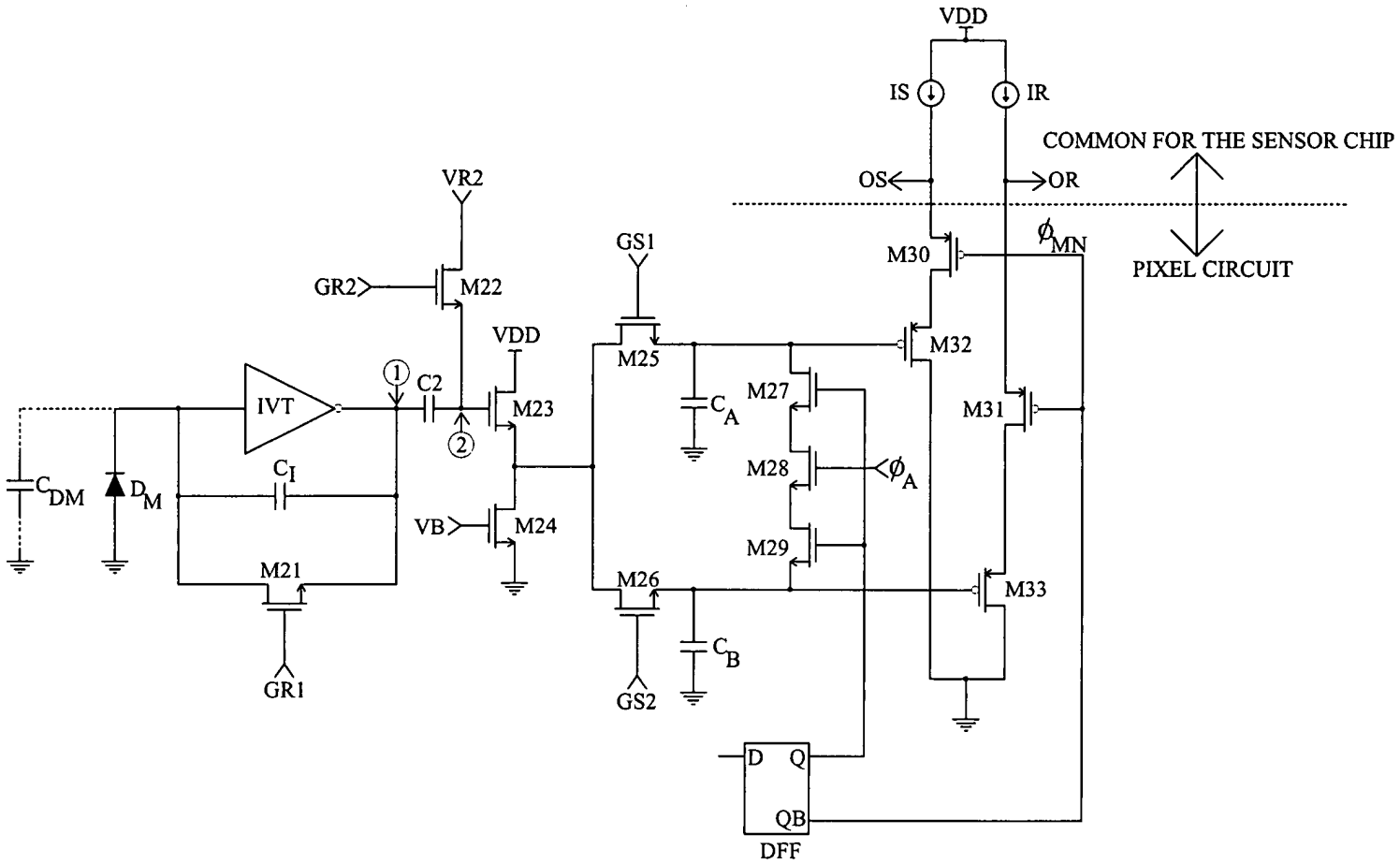
VDD
IS
IR
COMMON FOR THE SENSOR CHIP
OS
OR
PIXEL CIRCUIT
VR2
GR2
M22
GS1
M30
ϕ_{MN}
M25
M32
VDD
M23
M27
M31
IVT
C2
C_A
M28
ϕ_A
C_{DM}
D_M
C_I
VB
M24
M29
M21
M26
M33
C_B
GR1
GS2
D
Q
QB
DFF

FIG. 11A

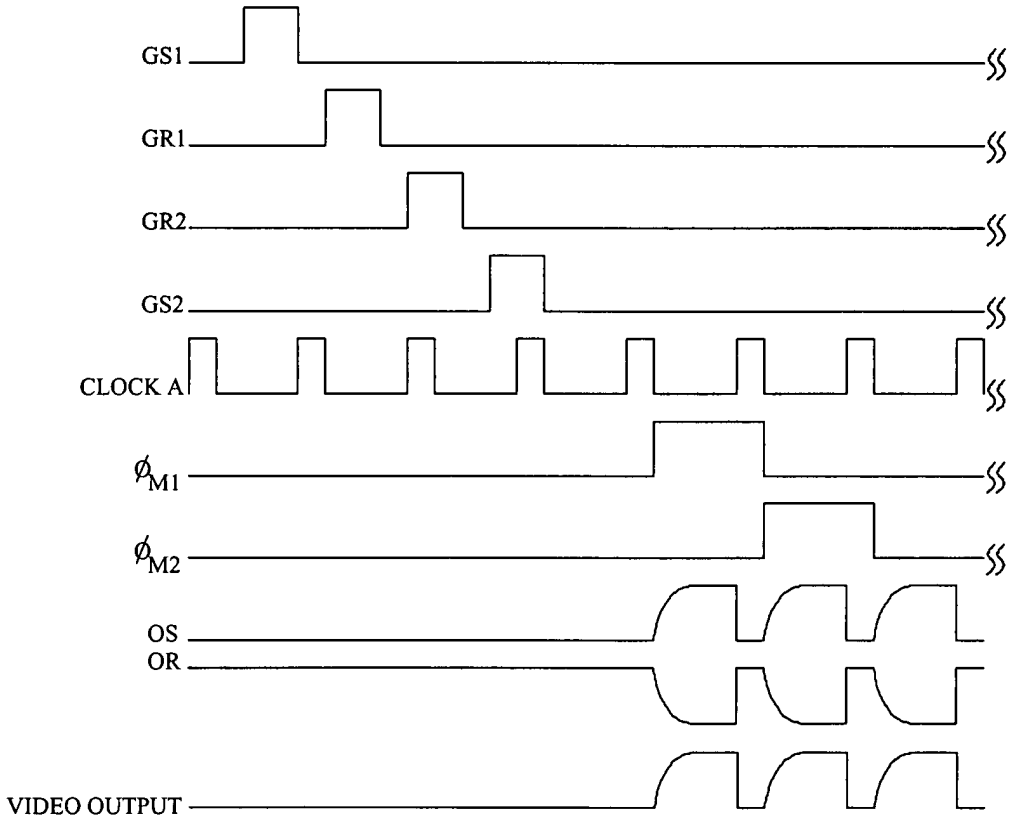

FIG. 11B

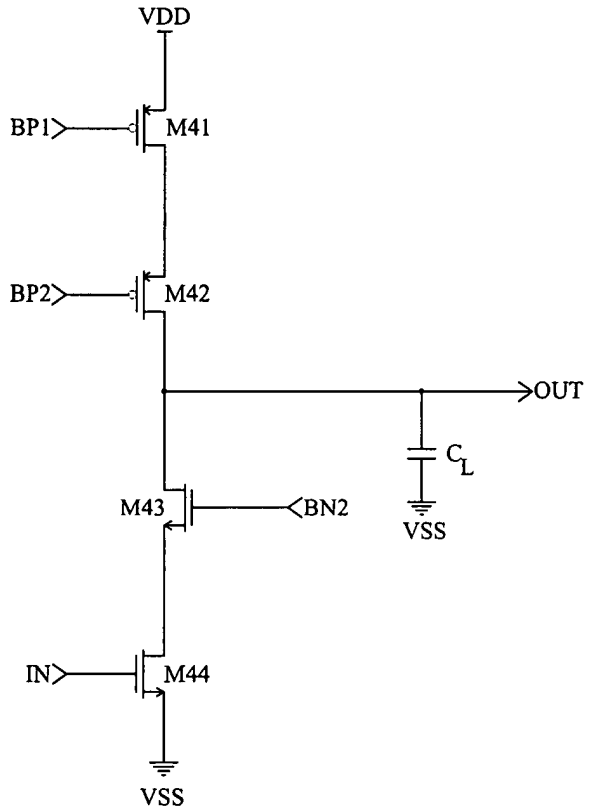

FIG. 12

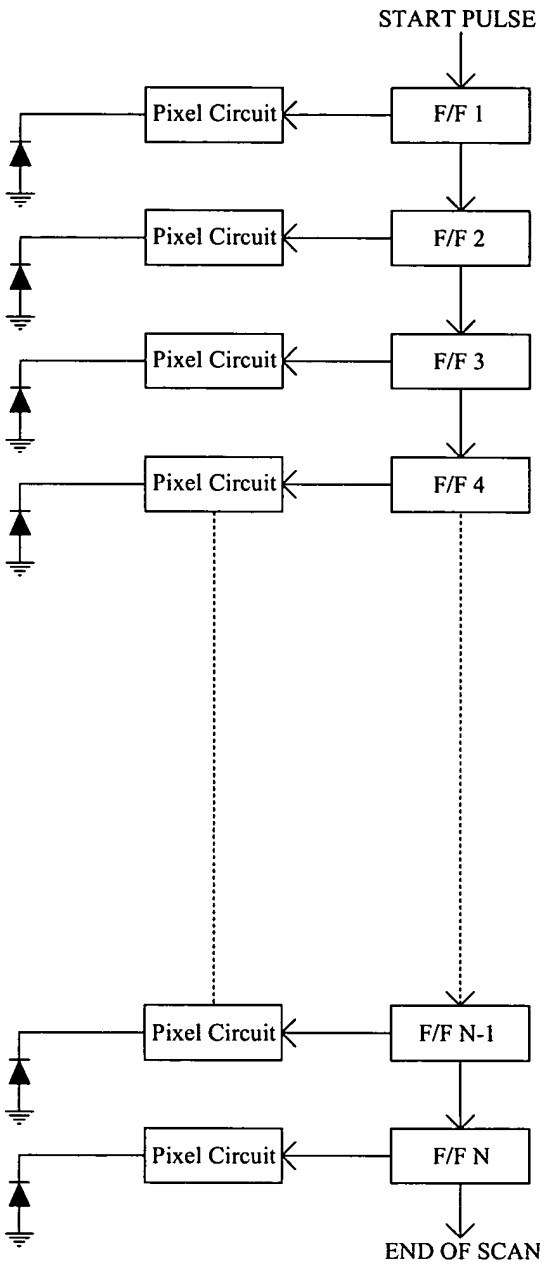
START PULSE
Pixel Circuit
F/F 1
Pixel Circuit
F/F 2
Pixel Circuit
F/F 3
Pixel Circuit
F/F 4
Pixel Circuit
F/F N-1
Pixel Circuit
F/F N
END OF SCAN

FIG. 13A

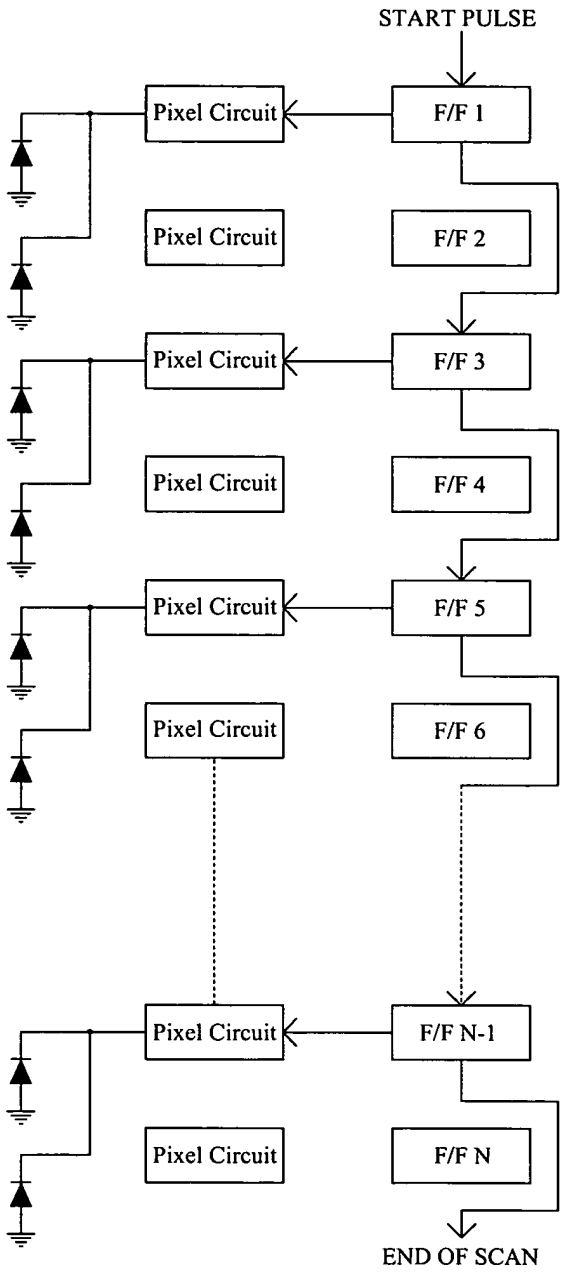
START PULSE
Pixel Circuit
F/F 1
Pixel Circuit
F/F 2
Pixel Circuit
F/F 3
Pixel Circuit
F/F 4
Pixel Circuit
F/F 5
Pixel Circuit
F/F 6
Pixel Circuit
F/F N-1
Pixel Circuit
F/F N
END OF SCAN

FIG. 13B

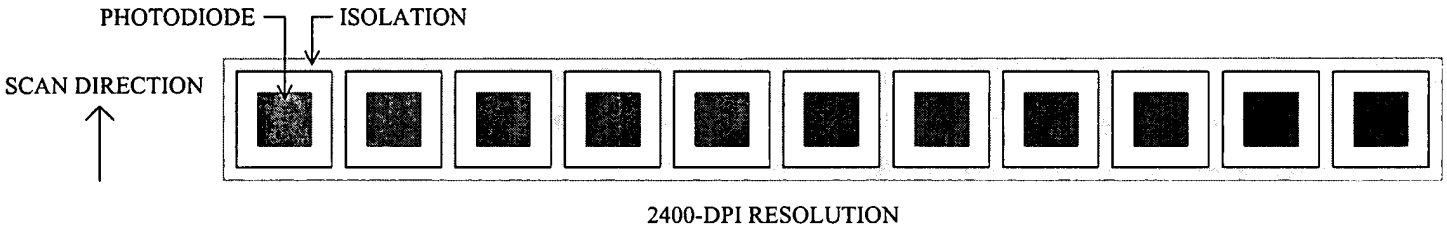

FIG. 14A
(PRIOR ART)

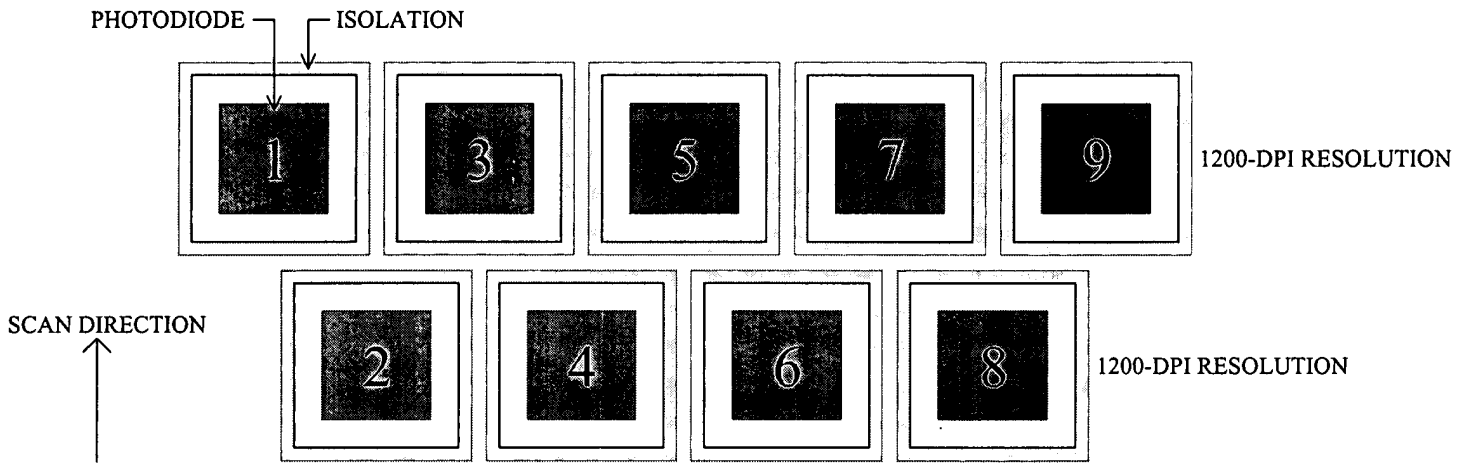
PHOTODIODE
ISOLATION
1
3
5
7
9
1200-DPI RESOLUTION
SCAN DIRECTION
2
4
6
8
1200-DPI RESOLUTION

FIG. 14B

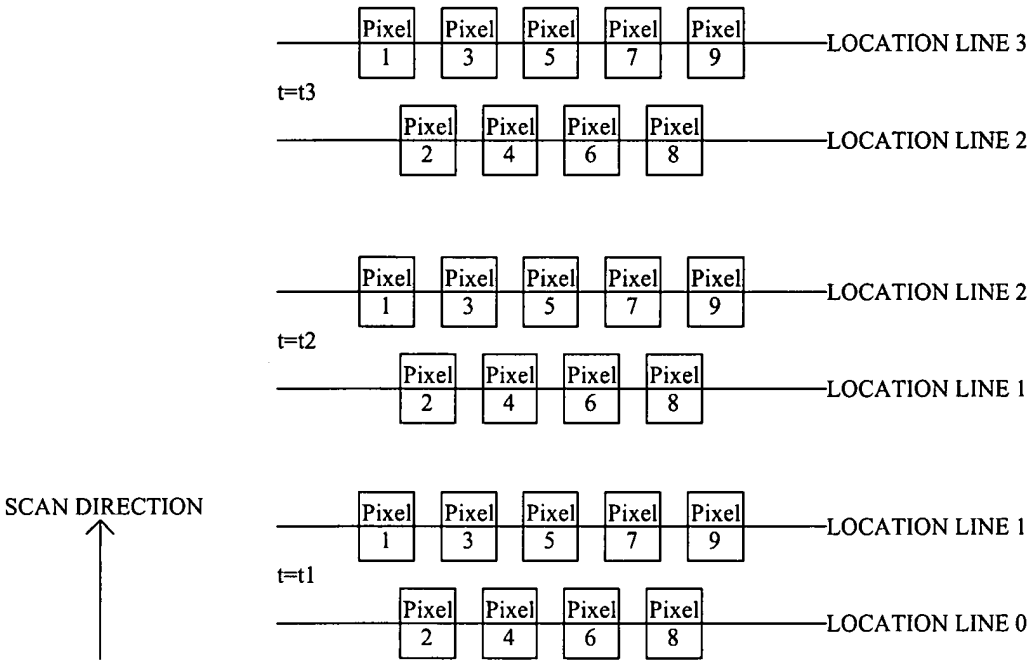
Pixel 1
Pixel 3
Pixel 5
Pixel 7
Pixel 9
LOCATION LINE 3
t=t3
Pixel 2
Pixel 4
Pixel 6
Pixel 8
LOCATION LINE 2
Pixel 1
Pixel 3
Pixel 5
Pixel 7
Pixel 9
LOCATION LINE 2
t=t2
Pixel 2
Pixel 4
Pixel 6
Pixel 8
LOCATION LINE 1
SCAN DIRECTION
Pixel 1
Pixel 3
Pixel 5
Pixel 7
Pixel 9
LOCATION LINE 1
t=t1
Pixel 2
Pixel 4
Pixel 6
Pixel 8
LOCATION LINE 0

FIG. 15A

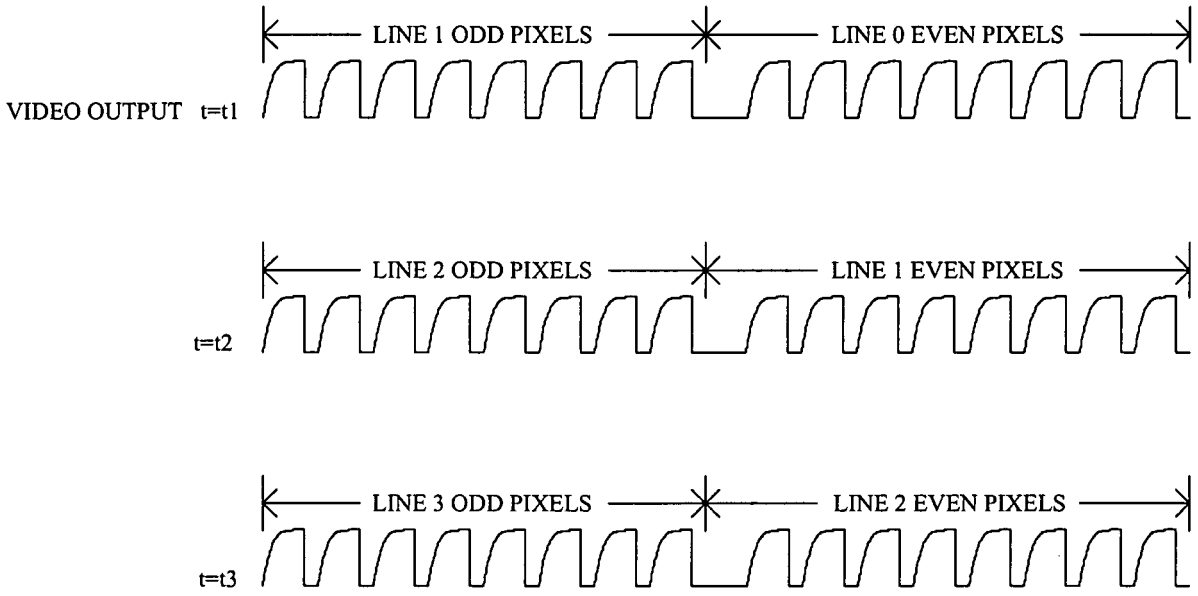
LINE 1 ODD PIXELS
LINE 0 EVEN PIXELS
VIDEO OUTPUT t=t1
LINE 2 ODD PIXELS
LINE 1 EVEN PIXELS
t=t2
LINE 3 ODD PIXELS
LINE 2 EVEN PIXELS
t=t3

FIG. 15B

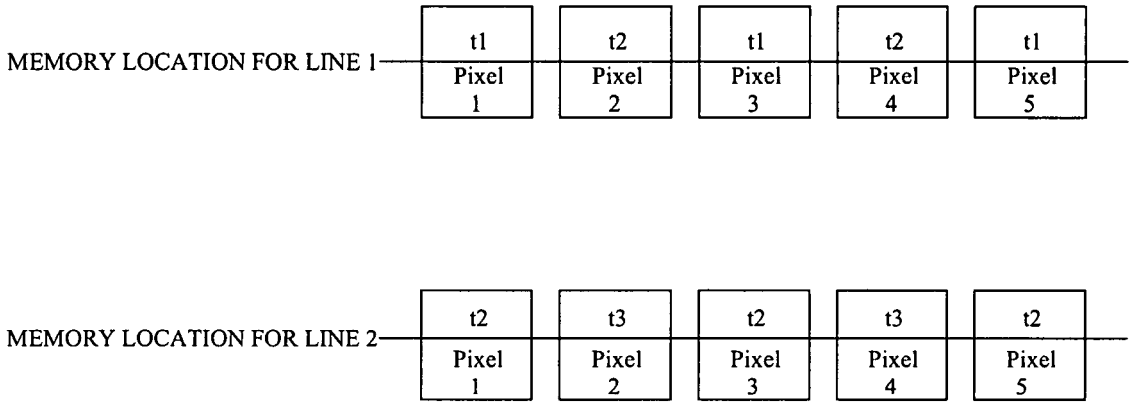
MEMORY LOCATION FOR LINE 1
t1
Pixel 1
t2
Pixel 2
t1
Pixel 3
t2
Pixel 4
t1
Pixel 5
MEMORY LOCATION FOR LINE 2
t2
Pixel 1
t3
Pixel 2
t2
Pixel 3
t3
Pixel 4
t2
Pixel 5

FIG. 15C